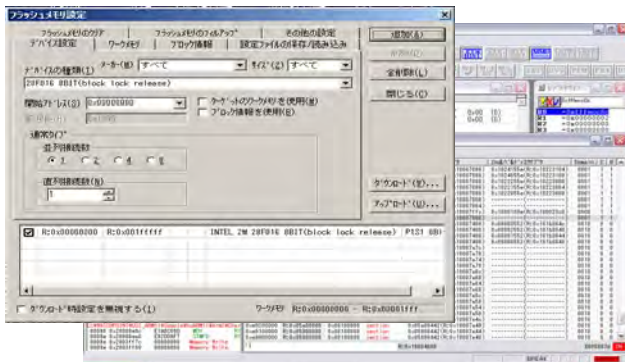


Multi-Core Tensilica Xtensa EJ-SCT Universal JTAG Emulator with WATCHPOINT Debugger



- Debug up to 10 Tensilica Xtensa LX cores with a single JTAG connection.
- Designed for the Tensilica JTAG interface.
- Diamond Standard support
- Supports Tensilica licensed XtensaLX2
- TIE and FLIX instructions are supported
- 4 Hardware break points, 2 instruction, 2 data
- Unlimited software breakpoints
- Read & Write FLASH in manual or macro mode
- Small and USB powered make it perfect for on-site debug or firmware updates.
- Stand-alone FLASH programming without a PC - DC power supply needed for this mode.
- Recorded or text macros execute at a touch of the button on the JTAG pod. Perfect for test, field firmware updates, and small run production programming with or without a PC connection.
- Multiple EJ-SCT may be chained together for FLASH programming use.
- Supports all RTOS compliant with TOPPERS μITRON (Ver. 4.0) specification
- Includes Watchpoint debugger for Windows® 2000 and XP operating systems

Specifications

Target CPU	T1020, T1030, T1040, T1050, Xtensa LX, Xtensa6 ⁺³ , Xtensa7, Xtensa LX2 Diamond Standard Processors (Supports the ASIC with the on-chip debugging interface)
Target Vcc	Vcc= +1.8 V to 3.6 V
Memory and I/O	Entire space is available to user
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	<ul style="list-style-type: none"> • Execution address break options: • Hardware breakpoints (Instruction address: 2 points, Data address: 2 points)* • Execution instruction address and memory access can be set. * The number of hardware breakpoints is specified when configuring the CPU. * Upon configuring the CPU, 2 instruction and 2 data access addresses must be specified. • Unlimited software breakpoints • The WATCHPOINT debugger can also force code execution to break.
Flash Memory	Download to target external Flash memory

- Note1: Max 10 CPUs can be debugged simultaneously. However, CPU configuration and user design may limit the number of cores that can be debugged at the same time.
- Note2: Supports the ASIC that includes Diamond Standard Processors and the on-chip debugging interface.
- Note3: The EJ-Debug for Xtensa LX supports Xtensa6, Diamond Standard Processors, but does not support the MMU capability of these processors
- Note4: Xtensa LX trace – WATCHPOINT debugger supports this feature. Contact us for additional technical information.

Supported Compiler - Tensilica C

OS Support

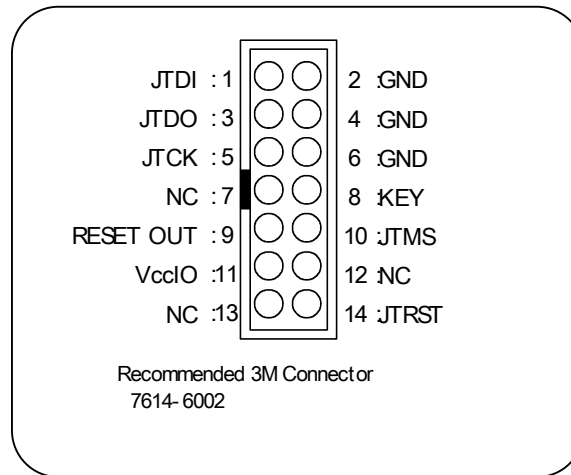
Windows CE, Linux

Note. Additional Link & Sync Watchpoint plug-in software is available for WinCE and Linux IDE sessions.

WinCE plug-in - Part number U43413

Linux IDE plug-in - Part number U42499

Target Connection - JTAG CABLE type SCP8000



14-pin JTAG Interface Connector Pin Assignment (Top View)

Ordering

Part number **SCD-SCM0801E**

PC Requirements

Windows98, Me, 2000, or XP

Memory: 32 Mbyte (64 Mbyte recommended)

Watchpoint installation requires 20 Mbyte drive space

Sophia
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Model numbers and specifications are subject to change without notice.